AMENDMENTS TO THE DRAWINGS:

Three replacement sheets of drawings are attached to this paper and include changes to Figs. 4, 5F, and 6. No changes were made to Figs. 5D-5E. The changes to Figs. 4, 5F, and 6 are discussed below in the remarks.

The replacement sheet containing Fig. 4 replaces the original sheet containing Fig. 4 filed with the application on February 8, 2002.

The replacement sheet containing Figs. 5D-5F replaces the original sheet containing Figs. 5D-5F filed with the application on February 8, 2002.

The replacement sheet containing Fig. 6 replaces the original sheet containing Fig. 6 filed with the application on February 8, 2002.

REMARKS

In accordance with the foregoing, the specification, Figs. 4, 5F, and 6, and claim 22 have been amended, and new claims 26-27 have been added. Claims 1-11, 13, 17-21, and 23 were previously canceled. Claims 12, 14-16, 22, and 24-27 are pending, with claims 12 and 22 being independent. Claims 12, 14-16, 22, and 24-25 are under consideration as being directed to the elected invention of Group I. New claims 26-27 are directed to the elected invention of Group I, and it is respectfully requested that new claims 26-27 be considered. No new matter is presented in this amendment.

The specification has been amended to improve its form.

Fig. 4 has been amended to change the direction of the cross-sectional view indicated by line V-V to be consistent with the cross-sectional views in Figs. 5A-5F.

Fig. 5F has been amended to indicate that the layers 320 and 330 end near the ends of layer 310 to be consistent with the plane view along line V-V in Fig. 4 and paragraph [0073], lines 3-4, of the specification.

Fig. 6 has been amended to add reference numerals 175-2 and 178 referred to in paragraph [0063], line 1, and paragraph [0066], line 1, of the specification.

Claim 22 has been amended solely to correct a typographical error in paragraph 4 wherein "one of the end portions" should be "ones of the end portions" to be consistent with "the ones of the end portions" in paragraph 8. It is submitted that this change to claim 22 does not add any new limitations to claim 22, such that it would not be proper for the Examiner to make the next Office Action final if that Office Action should include any new ground of rejection of claim 22.

New claims 26-27 respectively depending from independent claims 12 and 22 have been added to recite further features of the present invention.

Claim Rejections Under 35 USC 103(a)

Claims 12, 14, 22, and 25

Claims 12 ,14, 22, and 25 were rejected under 35 USC 103(a) as being unpatentable over Yoneda et al. (Yoneda) (U.S. Patent No. 5,837,568) in view of Yamazaki et al. '502 (Yamazaki '502) (U.S. Patent Application Publication No. 2003/0207502) and either Yamazaki et

al. '288 (Yamazaki '288) (U.S. Patent No. 5,568,288) or Teramoto et al. (Teramoto) (U.S. Patent No. 5,897,344). This rejection is respectfully traversed.

Claim 12

The Examiner considers glass substrate 10 in Fig. 13 of Yoneda to be "a substrate" as recited in claim 12; considers semiconductor layer 11 in Fig. 13 of Yoneda to be "a semiconductor layer formed over said substrate having end portions" as recited in claim 12; and considers gate insulation film 12 in Fig. 13 of Yoneda to be "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12.

However, it is submitted that Fig. 13 of Yoneda clearly shows that gate insulation film 12 does not expose ones of the end portions of semiconductor layer 11 as alleged by the Examiner, but rather covers ones of the end portions of semiconductor layer 11, specifically the end portions of source region 11S and drain region 11D which are at opposite ends of semiconductor layer 11.

Although Fig. 13 of Yoneda shows that gate insulation film 12 does expose portions of source region 11S and drain region 11D at contact holes CT2 and CT1 as shown in Fig. 12H of Yoneda, it is submitted that these exposed portions of source region 11S and drain region 11D cannot be considered to be end portions of semiconductor layer 11 because they do not include the ends of semiconductor layer 11. It is submitted that it is axiomatic that for a portion of a layer to be an end portion of a layer, that portion of the layer must necessarily include the end of the layer and a portion of the layer adjacent to the end of the layer.

Accordingly, for at least the reasons discussed above, it is submitted that Yoneda does not disclose "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12 as alleged by the Examiner. Nor is it seen where this feature of claim 12 is suggested by Yoneda.

The Examiner also apparently considers substrate 101 in Fig. 1 of Yamazaki '502 and glass substrate 301 in Fig. 3A of Yamazaki '502 to be "a substrate" as recited in claim 12; considers the active layer constituted by channel forming region 102, a pair of first impurity regions 103, a pair of second impurity regions 104, and a pair of third impurity regions 105 in Fig. 1 of Yamazaki '502 and active layers 303 and 304 in Fig. 3A of Yamazaki '502 to be "a semiconductor layer formed over said substrate having end portions" as recited in claim 12; and

considers gate insulating film 106 in Fig. 1 of Yamazaki '502 and gate insulating film 305 in Fig. 3A of Yamazaki '502 to be "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12.

As can be seen in Fig. 1 of Yamazaki '502, gate insulating film 106 does not cover ones of end portions of the active layer constituted by regions 102, 103, 104, and 105, specifically regions 105 which are at opposite ends of the active layer. However, the ones of the end portions of the active layer are in fact covered by silicon nitride film 108 which is an insulating layer as is well known in the art.

Also, as can be seen in Figs. 4C-4D of Yamazaki '502 which show the final steps of the method of manufacturing the CMOS circuit shown in Fig. 1 which begins with Fig. 3A, gate insulating film 305 does not cover ones of the end portions of the active layers 303 and 304. However, the ones of the end portions of active layers 303 and 304 are in fact covered by silicon nitride film 323 which is an insulating layer as is well known in the art.

The above interpretations of Yamazaki '502 are based on the applicants' position discussed above in connection with Yoneda that in order for a portion of a layer to be an end portion of a layer, that portion of the layer must necessarily include the end of the layer and a portion of the layer adjacent to the end of the layer.

It is submitted that the feature "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" recited in claim 12 indicates that ones of the end portions of a semiconductor layer not be covered by any insulating layer. Since ones of the end portions of the active layer in Fig. 1 of Yamazaki '502 are in fact covered by silicon nitride film 108 which is an insulating layer, and ones of the end portions of active layers 303 and 304 in Figs. 3A and 4C-4D of Yamazaki '502 are in fact covered by silicon nitride film 323 which is an insulating layer, it is submitted that Yamazaki '502 does not disclose "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12.

Accordingly, for at least the reasons discussed above, it is submitted that Yamazaki '502 does not disclose "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12 as alleged by the Examiner. Nor is it seen where this feature of claim 12 is suggested by Yamazaki '502.

Furthermore, since the Examiner considers Yoneda and Yamazaki '502 to disclose this feature of claim 12, the applicants will not speculate as to whether the Examiner may

alternatively consider this feature of claim 12 to be disclosed or suggested by Yamazaki '288 or Teramoto. However, should the Examiner take the position in the next Office Action that this feature of claim 12 is disclosed or suggested by Yamazaki '288 or Teramoto, it is submitted that this will constitute a new ground of rejection of claim 12, and accordingly the Examiner cannot make that Office Action final because claim 12 has not been amended in this paper.

The Examiner considers high-concentration source region 11S and high-concentration drain region 11D in Fig. 13 of Yoneda and second impurity regions 104 in Fig. 1 of Yamazaki '502 to be "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer," as recited in claim 12.

However, as discussed above, Yoneda and Yamazaki '502 do not disclose that the ones of the end portions of the semiconductor layer are exposed as recited in claim 12 because the end portions of the semiconductor layer are in fact covered by gate insulation film 12 as shown in Fig. 13 of Yoneda; by silicon nitride film 108 which is an insulating layer as shown in Fig. 1 of Yamazaki '402; and by silicon nitride layer 323 which is an insulating layer as shown in Figs. 4C-4D of Yamazaki '502.

Accordingly, it is submitted that Yoneda necessarily does not disclose "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer," as recited in claim 12 as alleged by the Examiner.

Furthermore, it is submitted that the language "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers" indicates that the entire portions of the semiconductor layer exposed beyond the spacers are formed to be high-density source and drain regions.

However, it is submitted that this is not the case in Yoneda as can be seen from Fig. 13 of Yoneda which shows that parts of the portions of the semiconductor layer exposed beyond spacers 15 are formed to be low concentration LD regions L11.

Furthermore, it is submitted that this is not the case in Yamazaki '502 as can seen from Fig. 1 of Yamazaki '502 which shows that parts of the portions of the semiconductor layer exposed beyond spacers 109 are formed to be medium-density impurity regions 104.

Although the Examiner has alleged that regions 104 in Fig. 1 of Yamazaki '502 are "high-density source and drain regions" as recited in claim 12, it is submitted that the Examiner's interpretation is incorrect in light of paragraphs [0056], [0058], and [0059] of Yamazaki '502 which state that first impurity regions 103 in Fig. 1 of Yamazaki '502 have an impurity concentration of typically between $5x10^{15}$ to $5x10^{16}$ atoms/cm^3; that second impurity regions 104 in Fig. 1 of Yamazaki '502 have an impurity concentration of typically between $1x10^{17}$ to $5x10^{18}$ atoms/cm^3; and that third impurity regions 105 in Fig. 1 of Yamazaki '502 have an impurity concentration of typically between $1x10^{20}$ to $5x10^{20}$ atoms/cm^3.

Thus, the impurity concentration of second impurity regions 104 is typically 2 to 1000 times the impurity concentration of first impurity regions 103, and the impurity concentration of third impurity regions 105 is typically 20 to 5000 times the impurity concentration of second impurity regions 104. In light of this, it is submitted that the only reasonable characterization of these impurity regions is that first impurity regions 103 are low-density source and drain regions, that second impurity regions 104 are medium-density source and drain regions, and that third impurity regions 105 are high-density source and drain regions.

Accordingly, for at least the reasons discussed above, it is submitted that Yoneda and Yamazaki '502 do not disclose "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer," as recited in claim 12 as alleged by the Examiner. Nor is it seen where this feature of claim 12 is suggested by Yoneda or Yamazaki '502, or is disclosed or suggested by Yamazaki '288 and Teramoto.

As recognized by the Examiner, Yoneda does not disclose "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12 because Fig. 13 of Yoneda shows that low concentration LD regions 11L are formed only partially at regions of the semiconductor layer under spacers 15. More specifically, low concentration LD regions 11L do not occupy the entire regions under spacers 15, and furthermore extend outside the regions under spacers 15.

However, the Examiner considers low-density first impurity regions 103 in Fig. 1 of Yamazaki '502 to be "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said

spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12, and is of the opinion that it would have been obvious to incorporate this feature into Yoneda's device "since the spacers would function as masking layers."

However, as can be seen from Fig. 1 of Yamazaki '502, low-density first impurity regions 103 extend under gate electrode 107, and thus are not "formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions" as recited in claim 12, and do not constitute "lightly doped drain (LDD) regions under said spacers" as recited in claim 12. The process of forming the ends of low-density first impurity regions 103 which extend under gate electrode 107 is shown in Fig. 3B of Yamazaki '502 and is described as follows in paragraph [0117] of Yamazaki '502:

> [0117] Also, the first impurity regions 308 and 309 are formed by using the gate wirings 306 and 307 as masks in a self-aligning manner. At this point an intrinsic polysilicon layer remains directly under the gate wirings 306 and 307, where channel forming regions 310 and 311 are formed. However, in practice, some amount will wrap around the inside of the gate wiring and be doped, resulting in a structure in which the gate wirings 306 and 307, and the first impurity regions 308 and 309 overlap. (See FIG. 3B.)

Furthermore, assuming *arguendo* that Yamazaki '502 does disclose the "low-density source and drain regions" feature of claim 12, it is submitted that the Examiner's position that it would have been obvious to incorporate this feature into Yoneda's device "since the spacers would function as masking layers" is an improper motivation under 35 USC 103(a) because Yoneda already uses spacers 15 as masking layers as shown in Fig. 12E of Yoneda and described as follows in column 13, lines 36-37 of Yoneda:

> Referring to FIG. 12E, using the gate electrode 13 and the side wall 15 as a mask, n-type impurity ions, such as phosphorus P, are doped into the exposed layers for the first time through ion implantation at the acceleration voltage 80 keV.

That is, since Yoneda already uses spacers 15 as masking layers, it is submitted that one of ordinary skill in the art would not have been motivated to incorporate low-density first impurity regions 103 in Fig. 1 of Yamazaki '502 into Yoneda's device "since the spacers would function as masking layers" as proposed by the Examiner.

Accordingly, for at least the reasons discussed above, it is submitted that Yamazaki '502 does not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12 as alleged by the Examiner.

As recognized by the Examiner, Yoneda and Yamazaki '502 do not disclose or suggest "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12. However, the Examiner considers this feature of claim 12 to be taught by either Yamazaki '288 or Teramoto, and is of the opinion that it would have been obvious to incorporate this aspect of this feature into Yoneda's device "since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto."

However, the motivation "since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto" identified by the Examiner is taken solely from Teramoto as can be seen, for example, from the abstract of Teramoto. It is not seen how this motivation taken from Teramoto has any applicability whatsoever to Yamazaki '288. Thus, the Examiner has not identified any motivation for one of ordinary skill in the art to incorporate the source and drain electrodes disclosed by Yamazaki '288 into Yoneda's device as the Examiner is required to do in a rejection under 35 USC 103(a) by MPEP 2143 which provides as follows (emphasis by underlining added):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. (Citation omitted.)

Accordingly, for at least the reasons discussed above, it is submitted that Yamazaki '288 does not suggest "source and drain electrodes which directly contact, respectively, and without

contact holes, said high density source and drain regions" as recited in claim 12 as alleged by the Examiner.

The method of forming source and drain electrodes 23 and 24 shown in Figs. 1A-1D of Teramoto which the Examiner considers to teach "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12 is designed to eliminate problems with the prior-art source and drain electrodes 70 and 71 shown in Figs. 6A-6B of Teramoto. Source and drain electrodes 70 and 71 in Fig. 6A of Teramoto are arguably similar to source and drain electrodes 18 and 17 in Fig. 13 of Yoneda. The problems with source and drain electrodes 70 and 71 in Fig. 6A of Teramoto are described as follows in column 1, line 59, through column 2, line 24, of Teramoto:

> When the contact holes for the source/drain regions 63, 65 are formed, if overetching is done, the portions surrounding the contact holes are overetched around the interface with the silicon oxide film 66. If aluminum electrodes 70 and 71 are subsequently formed, aluminum atoms diffuse to the surrounding etched portions. Sometimes, aluminum atoms diffuse close to the channel formation region 64, thus deteriorating the characteristics and the reliability of the TFT.
>
> On the other hand, where the distance 74 between the contact portion for the source/drain region and the channel formation region 64 is larger, the sheet resistance of the source/drain region poses problems. One conceivable method of solving this problem is to reduce the distance indicated by 74. However, the distance cannot be reduced greatly because of the accuracy of mask alignment. Especially, where the used substrate is made of glass, shrinkage of the glass substrate caused during a heating step presents problems. Hence, the accuracy of mask alignment results in serious problems. For example, if a glass substrate 10 cm or more square is heated to about 600° C., the substrate shrinks easily by about several micrometers. Therefore, the present situation is that the distance indicated by 74 contains a margin of approximately 20 μm.
>
> Where the problems with overetching caused during formation of the contact holes for the source/drain regions are considered, it is impossible to reduce the distance 74 by a great extent. As described thus far, the prior art TFTs suffer from two problems; (1) The formation of the contact holes for the source/drain regions presents problems; and (2) In association with (1), the contact holes cannot be formed close to the channel formation region; Consequently, the sheet resistance of the source/drain regions poses problems.

The method shown in Figs. 1A-1D of Teramoto solves these problems by (1) not forming contact holes, and (2) forming triangular insulators 22 which determine the positions at which source and drain electrodes 23 and 24 contact source and drain regions 17 and 19 and enable source and drain electrodes 23 and 24 to contact source and drain regions 17 and 19 closer to channel region 18.

The method shown in Figs. 1A-1D of Teramoto eliminates the need to form contact holes by using RIE (reactive ion etching) to etch away silicon oxide layer 21 and gate insulating film 14 shown in Fig. 1B, thereby forming triangular insulators 22 and exposing source and drain regions 17 and 19 as shown in Fig. 1C.

However, it is not seen how this method eliminates the potential for overetching that Teramoto claims to exist when contact holes are formed. When contact holes are formed as shown in Fig. 6A of Teramoto, it is necessary to etch away interlayer insulator 69 and gate insulating film 66 to expose source and drain regions 63 and 65, which appears to be basically the same as etching away silicon oxide layer 21 and gate insulating film 14 to expose source and drain regions 17 and 19 as shown in Figs. 1B-1C of Teramoto. It seems that the potential for overetching would exist in either case.

Contact holes CT2 and CT1 shown in Fig. 12H of Yoneda in which source and drain electrodes 18 and 17 are formed as shown in Fig. 12I of Yoneda are formed by RIE (reactive ion etching) as described in column 14, lines 59-61, of Yoneda, the same method used in Teramoto to etch away silicon oxide layer 21 and gate insulating film 14.

Since Yoneda's method and Teramoto's method both use the same etching method, it seems that the potential for overetching would exist in either case. In light of this, it is submitted that Teramoto's method would not provide any advantages over Yoneda's method, and accordingly it is submitted that one of ordinary skill in the art would not have been motivated to use Teramoto's method in Yoneda's device as proposed by the Examiner to eliminate the need to form contact holes in Yoneda's device.

Furthermore, if Teramoto's method were to be used in Yoneda's device, it appears that triangular insulators 22 in Fig. 1C of Teramoto would have to be formed on the portion of first interlayer insulation film 16 surrounding gate electrode 13, capping layer 14, and spacers 15 shown in Figs. 12H-12J of Yoneda. If this were done, it appears that triangular insulators 22 would extend to about the edge of contact holes CT2 and CT1, which would make it impossible

for source and drain electrodes 18 and 17 to be formed closer to channel region 11N, which is one of the asserted advantages of Teramoto's method.

Since it appears that using Teramoto's method in Yoneda's device would not result in Teramoto's asserted advantage of forming source and drain electrodes closed to a channel region, it is submitted that one of ordinary skill in the art would not have been motivated to use Teramoto's method in Yoneda's device as proposed by the Examiner.

For at least the reasons discussed above, it is submitted that Teramoto does not suggest "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12 as alleged by the Examiner.

For at least the reasons discussed above, it is submitted that Teramoto, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or suggest "a first insulating layer formed over said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12, or "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers" as recited in claim 12, or "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12, or "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12. Accordingly, it is submitted that claim 12 patentably distinguishes over Teramoto, Yamazaki '502, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 12 under 35 USC 103(a) as being unpatentable over Teramoto in view of Yamazaki '502 and either Yamazaki '288 or Teramoto be withdrawn.

Claim 14

Notwithstanding the position taken by the Examiner, it is noted that claim 14 depends from claim 12, and thus recites all of the features recited in claim 12 together with further features of the present invention. For at least the reasons discussed above in connection with claim 12, it is submitted that Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or suggest the features of claim 12 which are discussed above and are recited in claim 14 by virtue of its dependency from claim 12.

Accordingly, it is submitted that claim 14 patentably distinguishes over Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 14 under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '288 or Teramoto be withdrawn.

Claim 22

It is submitted that Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or suggest "a first insulating layer formed over said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 22, or "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers" as recited in claim 22, or "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers," as recited in claim 22, or "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 22 for at least the reasons discussed above that Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or suggest the same or similar features of claim 12. Accordingly, it is submitted that claim 22 patentably distinguishes over Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 22 under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '288 or Teramoto be withdrawn.

Claim 25

As recognized by the Examiner, Yoneda does not disclose or suggest "an organic electro-luminescence (EL) layer and a cathode electrode sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of said planarization layer" as recited in claim 25. However, the Examiner considers these features to be disclosed in Fig. 25 (presumably Fig. 25B) and paragraph [0343] of Yamazaki '502, although paragraph [0343] referred to by the Examiner relates to Fig. 26 of Yamazaki '502 and planarization layer 4142 referred to by the Examiner appears in Fig. 26. However, it is noted that Fig. 25B of Yamazaki '502 shows a similar planarization layer 4026.

In any event, the Examiner did not take the position that it would have been obvious to incorporate these features of Yamazaki '502 into Yoneda's device as the Examiner is required to establish a *prima facie* case of obviousness under 35 USC 103(a) with respect to claim 25, nor did the Examiner identify any motivation for such a combination of these references as the Examiner is required to do to establish a *prima facie* case of obviousness under 35 USC 103(a) with respect to claim 25.

In light of the Examiner's failure to establish a *prima facie* case of obviousness with respect to claim 25, it is submitted that it would not have been obvious to incorporate these features of Yamazaki '502 which relate to an electroluminescence (EL) display into Yoneda's device because Yoneda's device is a thin film transistor to be used in liquid crystal displays (LCDs) as described in column 1, lines 6-9, of Yamazaki '502.

Accordingly, for at least the reasons discussed above, it is submitted that claim 25 patentably distinguishes over Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 25 under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '288 or Teramoto be withdrawn.

Claims 15-16 and 24

Claims 15-16 were rejected under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '288 or Teramoto as applied to claim 12, and further in view of Yamazaki et al. '076 (Yamazaki '076) (JP 11-261076), and claim 24 was rejected under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '502 or Teramoto as applied to claim 22, and further in view of Yamazaki '076. These rejections are respectfully traversed.

Although the Examiner has referred to JP 11-261076 as "Yamazaki et al.", it is noted that Yamazaki is the last listed inventor. The first listed inventor is Fujimoto, such that it appears that JP 11-261076 should actually be referred to as "Fujimoto et al." However, the applicants will refer to this reference as "Yamazaki et al." as the Examiner has done.

Notwithstanding the position taken by the Examiner, it is noted that claims 15-16 depend from claim 12, and thus recite all of the features recited in claim 12 together with further features of the present invention. For at least the reasons discussed above in connection with claim 12, it is submitted that Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or

suggest the features of claim 12 which are discussed above and are recited in claims 15-16 by virtue of their dependency from claim 12. Nor is it seen where these features of claims 15-16 are disclosed or suggested by Yamazaki '076.

Furthermore, notwithstanding the position taken by the Examiner, it is noted that claim 24 depends from claim 22, and thus recites all of the features recited in claim 22 together with further features of the present invention. For at least the reasons discussed above in connection with claim 22, it is submitted that Yoneda, Yamazaki '502, Yamazaki '288, and Teramoto do not disclose or suggest the features of claim 22 which are discussed above and are recited in claim 24 by virtue of its dependency from claim 22. Nor is it seen where these features of claim 24 are disclosed or suggested by Yamazaki '076.

Accordingly, for at least the reasons discussed above, it is submitted that claims 15-16 and 24 patentably distinguish over Yoneda, Yamazaki '502, Yamazaki '288, Teramoto, and Yamazaki '076 in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claims 15-16 under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '288 or Teramoto as applied to claim 12, and further in view of Yamazaki et al. '076, be withdrawn, and that the rejection of claim 24 under 35 USC 103(a) as being unpatentable over Yoneda in view of Yamazaki '502 and either Yamazaki '502 or Teramoto as applied to claim 22, and further in view of Yamazaki '076, be withdrawn.

Claims 12 and 22

Claims 12 and 22 were rejected under 35 USC 103(a) as being unpatentable over Yoneda in view of Kim et al. (Kim) (U.S. Patent No. 6,706,569) and either Yamazaki '288 or Teramoto. This rejection is respectfully traversed.

Claim 12

For at least the reasons discussed above in connection with the other rejection of claim 12, it is submitted that Yoneda does not disclose "a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer" as recited in claim 12, or "high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer," as recited in claim 12 as alleged by the Examiner.

As recognized by the Examiner, Yoneda does not disclose "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12 because Fig. 13 of Yoneda shows that low concentration LD regions 11L are formed only partially at regions of the semiconductor layer under spacers 15. More specifically, low concentration LD regions 11L do not occupy the entire regions under spacers 15, and furthermore extend outside the regions under spacers 15.

However, the Examiner considers low-concentration impurity regions 1s' and 1d' in Fig. 11 (presumably Fig. 11B) of Kim to be "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12, and is of the opinion that it would have been obvious to incorporate this feature into Yoneda's device "since the spacers would function as implantation masks as taught by Kim."

However, as can be seen from Figs. 10B and 11B of Kim, low-concentration impurity regions 1s' and 1d' appear to extend under gate electrode 5, and thus are not "formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions" as recited in claim 12, and do not constitute "lightly doped drain (LDD) regions under said spacers" as recited in claim 12.

Furthermore, assuming *arguendo* that Kim does disclose the "low-density source and drain regions" feature of claim 12, it is submitted that the Examiner's position that it would have been obvious to incorporate this feature into Yoneda's device "since the spacers would function as implantation masks as taught by Kim" is an improper motivation under 35 USC 103(a) because Yoneda already uses spacers 15 as implantation masks as shown in Fig. 12E of Yoneda and described as follows in column 13, lines 36-37 of Yoneda:

> Referring to FIG. 12E, using the gate electrode 13 and the side wall 15 as a mask, n-type impurity ions, such as phosphorus P, are doped into the exposed layers for the first time through ion implantation at the acceleration voltage 80 keV.

That is, since Yoneda already uses spacers 15 as implantation masks, it is submitted that one of ordinary skill in the art would not have been motivated to incorporate low-

concentration impurity regions 1s' and 1d' in Fig. 11B of Kim into Yoneda's device "since the spacers would function as implantation masks as taught by Kim" as proposed by the Examiner.

Accordingly, for at least the reasons discussed above, it is submitted that Kim does not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12 as alleged by the Examiner.

As recognized by the Examiner, Yoneda and Yamazaki '502 do not disclose or suggest "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12. However, the Examiner considers this feature of claim 12 to be taught by either Yamazaki '288 or Teramoto, and is of the opinion that it would have been obvious to incorporate this aspect of this feature into Yoneda's device "since that would minimize source/drain sheet resistance and eliminate the need for performing mask alignment as taught by Teramoto."

However, for at least the reasons discussed above in connection with the other rejection of claim 12, it is submitted that Yamazaki '288 and Teramoto do not suggest "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12 as alleged by the Examiner.

Accordingly, for at least the reasons discussed above, it is submitted that Yoneda, Kim, Yamazaki '288, and Teramoto do not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers," as recited in claim 12, or "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 12. Accordingly, it is submitted that claim 12 patentably distinguishes over Yoneda, Kim, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 12 under 35 USC 103(a) as being unpatentable over Yoneda in view of Kim and either Yamazaki '288 or Teramoto be withdrawn.

Claim 22

It is submitted that Yoneda, Kim, Yamazaki '288, and Teramoto do not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers" as recited in claim 22, or "source and drain electrodes which directly contact, respectively, and without contact holes, said high density source and drain regions" as recited in claim 22 for at least the reasons discussed above that Yoneda, Kim, Yamazaki '288, and Teramoto do not disclose or suggest the same or similar features of claim 12. Accordingly, it is submitted that claim 22 patentably distinguishes over Yoneda, Kim, Yamazaki '288, and Teramoto in the sense of 35 USC 103(a), and it is respectfully requested that the rejection of claim 22 under 35 USC 103(a) as being unpatentable over Yoneda in view of Kim and either Yamazaki '288 or Teramoto be withdrawn.

New Claims 26-27

New claim 26 recites "[t]he TFT of claim 12, wherein said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer."

New claim 27 recites "[t]he active matrix display device of claim 22, wherein said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer."

Claims 26-27 depend from claims 12 and 22, and thus recite all of the features recited in claims 12 and 22 together with further features of the present invention. For at least the reasons discussed above in connection with claims 12 and 22, it is submitted that Yoneda, Yamazaki '502, Yamazaki '288, Teramoto, and Kim do not disclose or suggest the features of claims 12 and 22 which are discussed above and are recited in claims 26-27 by virtue of their dependency from claims 12 and 22. Nor is it seen where these features of claims 26-27 are disclosed or suggested by Yamazaki '076.

Furthermore, it is submitted that Kim does not disclose the feature of claims 26-27 "wherein said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer" because Fig. 11B of

Kim shows that low-concentration impurity regions 1s' and 1d' which the Examiner considers to be low-density source and drain regions do not extend through an entire thickness of semiconductor layer 1 in which they are formed. Nor is it seen where this feature of claims 26-27 is suggested by Kim.

For at least the reasons discussed above, it is submitted that claims 26-27 patentably distinguish over Yoneda, Yamazaki '502, Yamazaki '288, Teramoto, Kim, and Yamazaki '076, and an indication to that effect is respectfully requested.

Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this paper, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: 09/29/05

By: _____
Randall S. Svihla
Registration No. 56,273

1400 Eye St., NW
Suite 300
Washington, D.C. 20005
Telephone: (202) 216-9505
Facsimile: (202) 216-9510